

AMENDMENTS TO THE CLAIMS

1. (Currently amended): An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure S comprising:

a node set T;

an interconnect set I that selectively connects nodes in the node set T;

a device set A mutually exclusive of the node set T with ~~the devices~~ each device in the device set A ~~being capable of~~ sending data to one or more nodes in the node set T;

a device set Z mutually exclusive of the node set T with ~~the devices~~ each device in device set Z ~~being capable of~~ receiving data from one or more nodes in the node set T; and

a collection C of node subsets of the node set T, each node in the node set T being contained in exactly one member of the collection C such that:

for a device x in the device set Z, a sequence $cx = cx_0, cx_1, cx_2, \dots, cx_j$ exists with each member of the sequence cx being a node set in the collection C, the sequence cx ~~being capable of~~ passing data from devices in the device set A to the device x on a plurality of paths, among the plurality of paths being a path set P(x) characterized in that a path R is included in the path set P(x) only if each node on the path R is in a member of the sequence cx, a node of the path R that receives a message directly from a device in the device set A being a member of node set cx_U and a node of the path R that sends data directly to the device x being a member of node set cx_V with U being larger than V;

for a member Y of the collection C, a corresponding set of devices Z(Y) exists in the device ~~plurality~~ set Z such that a device y is included in the set of devices Z(Y) only if the member Y is also a member of ~~[[the]]~~ a sequence cy;

for members cx_H and cx_K of the sequence cx with $H > K$, a device set $Z(cx_K)$ is a subset of a device set $Z(cx_H)$;

the sequence cx includes two members cx_L and cx_M with $L > M$ and with

~~[[the]]~~ a device set $Z(cx_M)$ being a subset of a device set $Z(cx_L)$ and

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a device exists in the device set $Z(cx_L)$ that is not included in the device set $Z(cx_M)$; and

the node set T includes three distinct nodes p , q , and r , the node p being in a member cx_D of the sequence cx , the nodes q and r being in a member cx_E of the sequence cx with $D > E$, in one path of the plurality of paths $P(x)$ a message moves directly from the node p to the node r and in another path of the plurality of paths $P(x)$ a message moves directly from the node q to the node r .

2. (Original): An interconnect structure according to Claim 1 wherein: the plurality of paths of the sequence cx include a path such that if a message hops from a node in a member cx_n to a node in a member cx_m , then $n > m$.

3. (Currently amended): An interconnect structure according to Claim 1 further comprising:
an arrangement of the nodes in the interconnect structure into a hierarchy of levels of node sets $LV = LV_0, LV_1, \dots, LV_J$, each member of the hierarchy LV being a node set that is subset of the node set T and each node in the node set T is contained in exactly one member of the node sets LV ; and
for the device x of the device set Z , a node set cx_N is a subset of $[[the]]$ a level N node set L_N , with N not exceeding J .

4. (Currently amended): An interconnect structure according to Claim 3 wherein:

the collection C includes 2^{J-N} members on a level N ;

the collection C includes three members D , E and F such that member node set D is on $[[the]]$ a level LV_N and member node sets E and F are on $[[the]]$ a level LV_{N-1} ;

the interconnect set I includes interconnects positioned to allow data to pass directly from the member node set D to the member node set E and to pass directly from the node set D to the node set F ; and

the device set Z includes device sets $Z(D)$, $Z(E)$, and $Z(F)$ that correspond to the three members D , E , and F , the device sets $Z(E)$ and $Z(F)$ being mutually

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exclusive device sets, and the device set $Z(D)$ is the union of the device sets $Z(E)$ and $Z(F)$.

5. (Currently amended): An interconnect structure according to Claim 1 further comprising:

a logic L_p associated with the node p wherein for a message M_p that arrives at the node p , the logic L_p uses information concerning the sending of messages from the node q for the logic L_p to determine where the node $[[pis]]$ p is to send the message M_p .

6. (Currently amended): An interconnect structure according to Claim 1 wherein:

the node q has priority over the node p to send data to the node r so that a message M_q located at the node q is not blocked from being sent to the node r by a message M_p at the node p ; and

the node q ~~is capable of sending~~ sends a control signal to the node p wherein the purpose of the control signal is to enforce the priority of the node q over the node p to send data to the node r .

7. (Currently amended): An interconnect structure according to Claim 1 wherein:

the node set T includes a node s distinct from the nodes p , q , and r , the node s being in the member cx_D , so that in one path of the plurality of paths $P(x)$, a message moves from the ~~node P~~ node p directly to the node s .

8-13. (Canceled).

14. (Currently Amended): An interconnect structure according to Claim 8 comprising:

a plurality of nodes including a node N_E and a node set P , the node set P including a plurality of nodes that send data to the node N_E ; and
a plurality of interconnect paths interconnecting the plurality of nodes, the interconnect paths including data interconnect paths that couple nodes in

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pairs, a node pair including a sending node and a receiving node, the sending node sending data to the receiving node;

the nodes in the node set P having a priority relationship for sending data to the node N_E, the nodes in the node set P including distinct nodes N_F and N_A, the node N_F having a highest priority among the nodes in the node set P for sending data to the node N_E so that a message M_F arriving at the node N_F is not blocked from traveling to the node N_E by a message M_A arriving at the node N_A; and

for a message M arriving at the node N_A and the message M is blocked from being sent to the node N_E, then the blocking of the message M from being sent to the node N_E causes sending of the message M from the node N_A to a node distinct from the node N_E, wherein:

when a message M arrives at the node N_A and is targeted for the node N_E and not blocked by a message M' arriving at a node in the node set P having a higher priority than the node N_A for sending messages to the node N_E, the node N_A sends the message M to the node N_E.

15-23. (Canceled).

24. (Currently amended): An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure according to Claim 15 further comprising:

a node set T;

an interconnect set I that selectively connects nodes in the node set T;

a device set A mutually exclusive with the node set T with each device in the device set A sending data to a node in the node set T;

a device set Z mutually exclusive with the node set T with each device in the device set Z receiving data from a node in the node set T;

a set of data paths P, each path of the path set P carrying data from a device in the device set A to a device in the device set Z, each node on the path of the path set P is included in the node set T, and each interconnect in the path is included in the interconnect set I;

a node set U characterized as the set of nodes within the node set T that are on a path included in the path set P;

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for a node N in the node set T such that the node N is on a path in the path set P, a corresponding set of devices Z(N) exists in the device set Z such that a device w is included in the device set Z(N) only if a path exists in the path set P from a member of the device set A to the device w such that the path contains the node N;

the node set U includes three distinct nodes N_A , N_D , and N_E such that the node N_A sends data to the node N_D and the node N_E , and a device set $Z(N_A)$ is the same as a device set $Z(N_D)$, and a device set $Z(N_E)$ is a proper subset of the device set $Z(N_A)$;

an interconnect link IL in interconnect set I, the interconnect link IL being an interconnect link on a path in the path set P such that a corresponding set of devices Z(IL) exists in the device set Z such that a device w is included in the device set Z(IL) only if a path containing the interconnect link IL in the path set P exists from a device in the device set A to the device w; and
~~the node set U~~ node set U includes distinct nodes N_A , N_D , and N_E such that ~~the~~ node N_A is capable of sending sends data to the node N_D on a link L_{AD} , the node N_A ~~is capable of sending~~ sends data to the node N_E on a link L_{AE} , and ~~the device a device set $Z(L_{AE})$ is a proper subset of the device a device~~ subset $Z(L_{AD})$.

25-35. (Canceled).

36. (Currently amended): An interconnect structure S comprising:

a plurality of nodes including nodes N_A , N_D , and N_E ;

a plurality of interconnect lines selectively coupling the nodes in the structure S;

a plurality of devices in a device set I that is mutually exclusive of the plurality of nodes, the devices in the device set I ~~being capable of~~ sending data to one or more of the plurality of nodes; and

a plurality of devices in a device set Z that is mutually exclusive of the plurality of nodes, the devices in the device set Z ~~being capable of~~ receiving data from one or more of the plurality of nodes, the device set Z comprising a plurality of device subsets further comprising:

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a device subset T_A consisting of devices t_A such that a message can be sent from a device in the device set I through the node N_A to the device devices t_A ;

a device subset T_D consisting of devices t_D such that a message can be sent from a device in the device set I through the node N_D to the device devices t_D ; and

a device subset T_E consisting of devices t_E such that a message can be sent from a device in the device set I through the node N_E to the device devices t_E ;

wherein:

the node N_A ~~is capable of sending~~ sends data to the node N_D ;

the node N_A ~~is capable of sending~~ sends data to the node N_E ;

the devices in the device subset T_A are included in the device subset T_D ; and

a device t_A exists that is included in the device subset T_A and excluded from the device subset T_E .

37. (Currently amended): An interconnect structure S according to Claim 36 further comprising:

a logic L ~~capable of controlling that controls~~ passage of messages sent through the interconnect structure S, wherein:

a plurality of messages P can be sent to a plurality of nodes from a plurality of devices in the device set I;

the plurality of messages P includes a message M_A having a target device in the device subset T_A ; and

the logic L ~~is capable of routing~~ routes the message M_A through the node N_A to a device in the device subset T_A .

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38. (Currently amended): An interconnect structure S according to ~~Claim 36~~ Claim 37 wherein:

the message M_A has a header; and

the logic L ~~is capable of routing~~ routes the message M_A through the interconnect structure S using information in the header of the message M_A .

39. (Original): An interconnect structure S according to Claim 36 wherein:
the logic L is distributed among one or more nodes of the plurality of nodes;
the plurality of nodes includes a node N; and
logic of the logic L associated with the node N uses control signals to route
messages through the node N.

40. (Currently amended): An interconnect structure S containing a plurality of
nodes and a plurality of interconnects selectively coupling the nodes, the interconnect
structure S comprising:

- a node set T including three distinct nodes N_A , N_D , and N_E ;
- a device set I mutually exclusive of the node set T and containing devices ~~capable~~
~~of sending that send~~ data to at least one node in the node set T;
- a device set Z mutually exclusive of the node set T and containing devices ~~capable~~
~~of receiving that receive~~ data from at least one node in the node set T;
- a plurality of paths P ~~capable of carrying that carry~~ data through the interconnect
structure S to devices in the device set Z;
- a device subset T_A exists such that a message can be sent on a path in the ~~path-set~~
paths P from a device in the device set I through the node N_A ~~to the device~~
a device in the device subset T_A ;
- a device subset T_D exists such that a message can be sent on a path in the ~~path-set~~
paths P from a device in the device set I through the node N_D ~~to the device~~
a device in the device subset T_D ;
- a device subset T_E exists such that a message can be sent on a path in the ~~path-set~~
paths P from a device in the device set I through the node N_E ~~to the device~~
a device in the device subset T_E ;

whercin:

the node N_A ~~is capable of sending~~ sends data to the node N_D along a path in
the ~~path-set~~ paths P;

the node N_A ~~is capable of sending~~ sends data to the node N_E along a path in
the ~~path-set~~ paths P;

the devices in the device subset T_A are included in the device subset T_D ;

and

a device exists that is included in the device subset T_A that is not included
in the device subset T_E .

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41. (Original): An interconnect structure S according to Claim 40 further comprising:

a logic L_A associated with the node N_A controls data flow from the node N_A .

42. (Currently amended): An interconnect structure S containing a plurality of nodes and a plurality of interconnects selectively coupling the nodes, the interconnect structure S comprising:

a node set T including three distinct nodes N_A , N_C , and N_E ;

a device set I mutually exclusive of the node set T and containing devices ~~capable of sending that send~~ data to at least one node in the node set T;

a device set Z mutually exclusive of the node set T and containing devices ~~capable of receiving that receive~~ data from at least one node in the node set T;

a plurality of paths P ~~capable of carrying that carry~~ data through the interconnect structure S to devices in the device set Z;

a device subset T_A exists such that a message can be sent on a path in the ~~path-set paths~~ P from a device in the device set I through the node N_A to ~~the device a device~~ in the device subset T_A ;

a device subset T_C exists such that a message can be sent on a path in the ~~path-set paths~~ P from a device in the device set I through the node N_C to ~~the device a device~~ in the device subset T_C ;

a device subset T_E exists such that a message can be sent on a path in the ~~path-set paths~~ P from a device in the device set I through the node N_E to ~~the device a device~~ in the device subset T_E ;

wherein:

the node N_C ~~is capable of sending~~ sends data to the node N_E along a path in the ~~path-set paths~~ P;

the node N_A ~~is capable of sending~~ sends data to the node N_E along a path in the ~~path-set paths~~ P;

the devices in the device subset T_C are included in the device subset T_E ; and
a device exists that is included in the device subset T_A that is not included in the device subset T_E .

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43. (Original): An interconnect structure S according to Claim 42 further comprising:

a logic L_A associated with the node N_A controls data flow from the node N_A .

44. (Original): An interconnect structure S according to Claim 43 wherein: a message M arriving at the node N_A has a header and the logic L_A uses information in the header to decide where to send the message M.

45. (Original): An interconnect structure S according to Claim 43 wherein: the logic L_A uses information from the node N_C to decide where to send the message M.

46. (New): An interconnect apparatus, comprising:
a plurality of nodes; and
a plurality of interconnect lines selectively coupling the nodes in a multiple level structure, the multiple level structure being arranged to include:
a plurality of $J+1$ levels in a hierarchy of levels T arranged from a level T equal to 0 to a level T equal to J;
a plurality of 2^{J-T} rings in each level T; and
a plurality of $2^T K$ nodes in a ring.

47. (New): An apparatus according to Claim 46 wherein a node A on a level T greater than 0 and less than J has a plurality of interconnections including:

an input interconnection from a node B on the level T;
an input interconnection from a node C on a level T+1;
an output interconnection to a node D on the level T; and
an output interconnection to a node E on a level T-1.

48. (New): An apparatus according to Claim 47 wherein a node A on a level T greater than 0 and less than J has a plurality of interconnections including:

a control input interconnection from the node F on the level T-1; and
a control output interconnection to the node G on the level T+1.

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49. (New): An apparatus according to Claim 47 wherein a node A on a level T greater than zero and less than J has a plurality of interconnections further including:
 an input interconnection from a node H on a level T-2; and
 an output interconnection to a node I on a level T+2.

50. (New): An apparatus according to Claim 49 wherein a node A on a level T greater than zero and less than J has a plurality of interconnections further including:
 a control input interconnection from a node J on a level T+2; and
 a control output interconnection to a node K on a level T-2.

51. (New): An apparatus according to Claim 47 wherein at most one input interconnection of input connections B and C is active at one time.

52. (New): An apparatus according to Claim 47 wherein at most one output interconnection of output connections D and E is active at one time.

53. (New): An apparatus according to Claim 47 wherein messages communicated on the input interconnection from the node B on the level T have a higher priority than messages communicated on the input interconnection from the node C on the level T+1.

54. (New): An apparatus according to Claim 47 wherein:
 a series of $2^T K$ sequential node A to node D interconnections on the level T traverses each of $2^T K$ nodes on one ring once.

55. (New): An apparatus according to Claim 46 wherein the multiple level structure has a three-dimensional cylindrical topology in which each node has a location designated in three-dimensional cylindrical coordinates (r, θ, z) where radius r is an integer which specifies the cylinder number from 0 to J, θ is an integer which specifies the $2\theta\pi/K$ spacing of nodes around the circular cross-section of a cylinder from 0 to K-1, and height z is a binary integer which specifies distance along the z-axis from 0 to $2^I - 1$.

56. (New): An apparatus according to Claim 55 wherein:
 a node $A(r, \theta, z)$ is interconnected with an immediate predecessor node $B(r, (\theta-1) \bmod K, H(z))$ on level r for receiving message data;

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node $A(r, \hat{e}, z)$ is interconnected with a predecessor node $C(r+1, (\hat{e}-1) \bmod K, z)$ on level $r-1$ for receiving message data;

node $A(r, \hat{e}, z)$ is interconnected with an immediate successor node $D(r, (\hat{e}+1) \bmod K, h_r(z))$ on level r for sending message data;

node $A(r, \hat{e}, z)$ is interconnected with a successor node $E(r-1, (\hat{e}+1) \bmod K, z)$ on level $r-1$ for sending message data;

node $A(r, \hat{e}, z)$ is interconnected with a node $F(r-1, \hat{e}, H_r(z))$ on level $r-1$ for receiving a control input signal; and

node $A(r, \hat{e}, z)$ is interconnected with a node $G(r+1, \hat{e}, h_{r+1}(z))$ on level $r+1$ for sending a control output signal.

57. (New): An apparatus according to Claim 56 wherein:

height $z = [z_{J-1}, z_{J-2}, \dots, z_r, z_{r-1}, \dots, z_2, z_1, z_0]$ is converted to $h_r(z)$ on the level r by reversing the order of low-order z bits from z_{r-1} to z_0 into the form $z = [z_{J-1}, z_{J-2}, \dots, z_r, z_0, z_1, z_2, \dots, z_{r-1}]$;

adding 1 (modulus 2^r); and

reversing back the low-order z bits; and

height z is converted to $H_r(z)$ on the level r by

reversing the order of low-order z bits from z_{r-1} to z_0 into the form $z = [z_{J-1}, z_{J-2}, \dots, z_r, z_0, z_1, z_2, \dots, z_{r-1}]$;

subtracting 1 (modulus 2^r); and

reversing back the low-order z bits.

58. (New): An apparatus according to Claim 57 wherein:

height $z = [z_{J-1}, z_{J-2}, \dots, z_r, z_{r-1}, \dots, z_2, z_1, z_0]$ is converted to $h_r(z)$ on the level r by reversing the order of low-order z bits from z_{r-1} to z_0 into the form $z = [z_{J-1}, z_{J-2}, \dots, z_r, z_0, z_1, z_2, \dots, z_{r-1}]$;

adding J (modulus 2^J) in which J is an odd integer; and

reversing back the low-order z bits; and

height z is converted to $H_r(z)$ on the level r by

reversing the order of low-order z bits from z_{r-1} to z_0 into the form $z = [z_{J-1}, z_{J-2}, \dots, z_r, z_0, z_1, z_2, \dots, z_{r-1}]$;

subtracting J (modulus 2^J); and

reversing back the low-order z bits.

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59. (New): An apparatus according to Claim 55 wherein a node $A(J, \theta, z)$ on an outermost level J includes:

- a first interconnection with a device outside of the multiple level structure for receiving message data; and
- a second interconnection with a device outside of the multiple level structure for sending a control output signal.

60. (New): An apparatus according to Claim 55 wherein a node $A(0, \theta, z)$ on an innermost level 0 includes:

- a first interconnection with a device outside of the multiple level structure for sending message data; and
- a second interconnection with a device outside of the multiple level structure for receiving a control output signal.

61. (New): An apparatus according to Claim 55 wherein:
on a level T , one ring is spanned in 2^T passes through the angles θ from 0 to $K-1$ so that 2^T heights z designate one ring.

62. (New): An apparatus according to Claim 46 further comprising:
a plurality of devices coupled to the nodes of a level.

63. (New): An apparatus according to Claim 46 further comprising:
a plurality of devices coupled to the nodes of level 0 ; and
a plurality of interconnect lines coupling the plurality of devices to respective nodes in the level J .

64. (New): An apparatus according to Claim 63 wherein a device is coupled to a plurality of nodes in the level J .

65. (New): An apparatus according to Claim 46 wherein:
 W_T rings are interconnected on a level T ;
 W_{T-1} rings are interconnected on a level $T-1$; and

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the W_{T-1} rings on level T-1 are divided into W_T mutually exclusive collections (C_1, C_2, \dots, C_{W_T}) such that each of the rings in collection C_n of level T-1 receive messages from ring R_M of level T.

66. (New): A communication interconnect structure for transmitting messages, comprising:

- a plurality of nodes arranged in a structure including:
- a hierarchy of levels from a source level to a destination level;
- a plurality of nodes spanning a cross-section of a level; and
- a plurality of nodes in a cross-section span;
- a plurality of interconnect lines coupling the nodes in the structure including for a node N on a level L:
 - a message input interconnect line coupled to a node on a previous level L+1;
 - a message input interconnect line coupled to a node on the level L;
 - a message output interconnect line coupled to a node on a subsequent level L-1; and
 - a message output interconnect line coupled to a node on a subsequent level L-1.

67. (New): An interconnect structure according to Claim 66 further comprising:
 a control input interconnect line coupled to the node on the subsequent level L-1
 which is coupled to the message output interconnect line; and
 means for receiving a message on the control input interconnect line and, in
 accordance with the message, selectively transmitting a message on the
 message output interconnect line coupled to the subsequent level L-1 node or
 on the message output interconnect line coupled to the level L.

68. (New): An interconnect structure according to Claim 67 further comprising:
 a control output interconnect line coupled to the node on the previous level L+1
 which is coupled to the message input interconnect line;
 means for determining that a message is blocking the node N; and
 means for communicating via the control input interconnect line informing whether
 the node N is blocked.

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69. (New): An interconnect structure according to Claim 68 further comprising:
means for timing a message transmission time of a message transmitted from a level
to a subsequent level and for timing a control signal transmission time of a
control signal from a subsequent level to a level so that the control signal
arrives first at a node.

70. (New): An interconnect structure according to Claim 69 further comprising:
a control output interconnect line coupled to the node on the previous level L+1
which is coupled to the message input interconnect line;
means for determining that a message is blocking the node N; and
means for communicating via the control input interconnect line informing whether
the node N is blocked.

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